CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a gate electrode formed on the semiconductor substrate through a gate dielectric layer;

first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer.

2. A semiconductor device according to claim 1, wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric layer is between about 0.05 and 0.15 μm.

3. A semiconductor device according to claim 1, wherein a groove section is formed at a specified location in the semiconductor substrate, and the gate electrode is formed on a bottom surface of the groove section through the gate dielectric layer.

4. A semiconductor device according to claim 1, wherein the gate electrode is formed from at least one alloy that includes at least two constituents selected from the following group:

polycrystalline silicon, tungsten, tantalum, copper and gold.

5. A semiconductor device according to any one of claim 1, wherein an element isolation region is formed in the semiconductor substrate.

6. A semiconductor device according to claim 5, wherein the element isolation region is formed from a trench isolation groove and a dielectric layer embedded therein.

7. A semiconductor device according to claim 1, wherein the first and second impurity diffusion layers include an extension region.

8. A semiconductor device according to any one of claim 1, wherein a third impurity diffusion layer is formed in a portion immediately below the gate electrode in the semiconductor substrate.

9. A semiconductor device according to any one of claim 1, wherein a metal silicide layer is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer on an upper surface thereof.

10. A semiconductor device according to any one of claim 1, wherein the sidewall dielectric layer is formed from a material including, as a main component, silicon nitride, silicon oxide or a compound film thereof.

11. A semiconductor device according to any one of claim 1, wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

12. A semiconductor device according to any one of claim 1, wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and a film thickness that gradually reduces from a bottom thereof toward an upper surface thereof.

13. A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a first dielectric layer on a semiconductor substrate;

removing a part of the first dielectric layer and the semiconductor substrate to thereby form a groove at a specified position;

forming a sidewall dielectric layer on a side surface section of the groove using a second dielectric layer composed of a material different from the first dielectric layer;

forming a gate dielectric layer on a bottom surface of the groove;

embedding a conductive material into the groove and then removing the first dielectric layer until at least a surface of the semiconductor substrate is exposed to thereby form a gate electrode; and

introducing an impurity in the semiconductor substrate to thereby form first and second impurity diffusion layers in the semiconductor substrate with the gate electrode interposed between them.

14. A method for manufacturing a semiconductor device according to claim 13, wherein the groove and the sidewall dielectric layer are formed to

have a specified width and a specified film thickness, respectively, to form a width of the gate electrode to have a specified length.

15. A method for manufacturing a semiconductor device according to claim 13, and further comprising:

forming an element isolation region at a specified location in the semiconductor substrate.

16. A method for manufacturing a semiconductor device according to claim 15, and:

wherein forming the element isolation region includes forming a trench isolation groove at a specified location on the semiconductor substrate before the first dielectric layer is formed;

wherein forming the first dielectric layer on the semiconductor substrate includes embedding the first dielectric layer in the trench isolation groove; and

wherein removing the first dielectric layer includes etching the first dielectric layer to thereby form an element isolation region embedded in the semiconductor substrate.

17. A method for manufacturing a semiconductor device according to any one of claim 13, and further comprising:

introducing an impurity into a region at a bottom surface of the groove in the semiconductor substrate to form a third impurity diffusion layer.

18. A method for manufacturing a semiconductor device according to claim 17, wherein introducing the impurity into the region at the bottom surface of the groove includes introducing an impurity of a first conduction type to form the third impurity diffusion layer; and further comprising:

introducing an impurity of a second conduction type into the third impurity diffusion layer formed of the impurity of the first conduction type to form a fourth impurity diffusion layer.

19. A method for manufacturing a semiconductor device according to claim 13, and further comprising:

forming a metal silicide layer on the first and second impurity diffusion layers, and forming a metal silicide layer on a top surface of the gate electrode.

20. A method for manufacturing a semiconductor device according to claim 13, wherein forming a sidewall dielectric layer on a side surface section of the groove includes:

forming a second dielectric layer over the surface of the semiconductor substrate; and

forming the side wall dielectric layer by anisotropically etching back the second dielectric layer,

wherein the second dielectric layer is formed of a material having an etching rate different from the etching rate of the first dielectric layer.